

29/6/2016

4E2149

Roll No. _____

Total No of Pages: 4

4E2149

B.Tech. IV-Sem (Main & Back) Exam; June-July 2016

Bio Medical Engineering

4BM3 Digital Electronics

BM, EX, EI, EC

Time: 3 Hours

Maximum Marks: 80

Min. Passing Marks (Main & Back): 26

Min. Passing Marks (Old Back): 24

Instructions to Candidates:-

Attempt any five questions, selecting one question from each unit. All Questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.

Units of quantities used/ calculated must be stated clearly.

Use of following supporting material is permitted during examination.

(Mentioned in form No.205)

1. _____

2. _____

UNIT-I

Q.1 (a) Perform the following operations-

[4×3 =12]

- (i) $(68)_{10} - (31)_{10}$ using BCD subtraction.
- (ii) $(1101101 - 1010111)_2$ using 1's complement method.
- (iii) $(22 - 31)_{10}$ using 9's complement method.
- (iv) $(1101101)_{\text{Gray}} \rightarrow ()_2$.

(b) Write a short note on error correction & detection codes.

[4]

OR

Q.1 (a) Simplify the

[4×2=8]

(i) $\overline{A}\overline{B} + ABC + A(B + \overline{A}\overline{B})$

(ii) $[A\overline{B}(C+BD) + \overline{A}\overline{B}]C$

(b) Find the value of x

[2+2 = 4]

(i) $(23)_x + (12)_x = (101)_x$

(ii) $(1000)_x = (11_2)^3$

(c) Implement Boolean function $f = (w + \overline{x})(w + \overline{x} + z)(y + \overline{z})$ using NOR gate only. [4]

UNIT-II

Q.2 (a) What do you understand by TTL logic. How open collector TTL is different from normal TTL circuit.

[6+4=10]

(b) Write down the comparison between CMOS & TTL families.

[6]

OR

Q.2 (a) Draw & explain the working of DTL- NAND gate.

[6]

(b) Explain the construction & operation of MOSFET. Implement the NAND & NOR gate using NMOS logic circuit.

[4+6=10]

UNIT-III

Q.3 (a) Obtain & realize the minimum SOP expression by using K map for $f(A, B, C, D)$

$$= \pi M(0, 2, 5, 7, 8, 10) \quad [8]$$

(b) Write a short note on variable mapping. [4]

(c) Develop the truth table for. [4]

$$f = \overline{A}B\overline{C}\overline{D} + \overline{A}BC\overline{D} + A\overline{B}\overline{C}D + \overline{A}\overline{B}C\overline{D}$$

OR

Q.3 (a) By using Quine- McCluskey method minimize the given output function. [8]

$$f = \Sigma_m(0, 1, 4, 7, 8, 10, 12, 13, 14) + \Sigma_d(5, 9)$$

(b) $ABC + \overline{A}BC + \overline{A}B\overline{C} + A\overline{B}\overline{C}$ Convert into POS form. [4]

(c) Convert $f = \overline{A}B + \overline{C} + AB\overline{D}$ into canonical SOP form. [4]

UNIT-IV

Q.4 (a) Draw & explain the logic diagram of binary Adder & subtractor. [8]

(b) Write a short note on Diode switching matrix. [8]

OR

Q.4 (a) Design the combinational logic circuit for BCD to EX-3 code converter. [8]

(b) Implement the following: [4×2=8]

(i) Full adder using half adder only

(ii) $f(A, B, C) = \pi M(0, 4, 6, 7)$ using 8:1 M_{ux}

UNIT-V

Q.5 (a) Draw the four bit binary ripple counter diagram using flip –flop that trigger on the positive edge. [8]

(b) Realization of [4×2=8]

(i) RS FF to JK FF

(ii) JK FF to D FF

OR

Q.5 (a) What do you understand by race around condition. How it over come in master slave JK FF. [8]

(b) Write a short note on shift registers. [8]
