

29/6/2016

4E2110

Roll No. _____

Total No of Pages: **3**

4E2110

B.Tech. IV-Sem (Back) Exam; June-July 2016

Electrical Engineering
4EE2(O) Digital Electronics

Time: 3 Hours

Maximum Marks: 80

Min. Passing Marks (Main & Back): 26

Min. Passing Marks (Old Back): 24

Instructions to Candidates:-

Attempt any five questions, selecting one question from each unit. All Questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.

Units of quantities used/ calculated must be stated clearly.

Use of following supporting material is permitted during examination.

(Mentioned in form No.205)

1. _____

2. _____

UNIT-I

Q.1 (a) Convert the following into the Gray number.

[9]

(i) $3A7_{16}$

(ii) 527_8

(iii) 652_{10}

(b) Perform the following decimal Subtraction in BCD by the 9's complement methods.

[5]

(i) $305.5 - 168.8$

(ii) $679.6 - 885.9$

(c) Convert 756.603_8 to hex.

[2]

OR

- Q.1 (a) Perform following: [6]
- (i) Multiply 1101_2 by 110_2
 - (ii) Divide 110101.11_2 by 101_2
- (b) Convert 2598.675_{10} to hex. [3]
- (c) Solve the following subtraction in XS – 3 code. [5]
- (i) $267 - 175$
 - (ii) $57.6 - 27.8$
- (d) Encode data bits 1101 into the 7 bit even – parity hamming code. [2]

UNIT-II

- Q.2 (a) Show that $(A+B) \overline{AB}$ is equivalent to $A \oplus B$. Also construct the corresponding logic diagrams. [5]
- (b) Reduce the expression $f = (B+BC) (B+\overline{B}C) (B+D)$ [4]
- (c) Reduce using mapping the expression. [7]
- $f = \sum m (2, 3, 6, 7, 8, 10, 11, 13, 14)$

OR

- Q.2 (a) Reduce the expression $f = \sum m (1, 5, 6, 12, 13, 14) + d (2,4)$ and implement the real minimal expression in universal logic. [12]
- (b) Implement the following function using only NOR gates. [4]
- $f = a (b + cd) b \overline{c}$

UNIT-III

- Q.3 (a) Give the definitions of voltage and current levels corresponding to the logic 'O' and logic 'I' states, as follows: - [4]
- $V_{IH} (min), V_{OH} (min), V_H (max), V_{IL} (max), V_{OL} (max), I_{IH}, I_{OH}, I_{OL}$
- (b) Draw and explain the working of two – input TTL (NAND) Gate. What is totem-pole output? Explain its advantages and disadvantages. [12]

OR

- Q.3 (a) Draw and explain the working of two input ECL OR /NOR gate. [8]
(b) Show the circuit diagram of two – input CMOS NAND gate and describe it. [8]

UNIT-IV

- Q.4 (a) Implement the following function using 8 – to -1 MUX [8]
$$f(x, y, z) = \sum m(0, 2, 3, 5)$$

(b) Sketch the logic diagram of 2 bit magnitude comparator and briefly explain its operation. [8]

OR

- Q.4 (a) Design the 4 input priority encoder with truth table and draw its logic diagram. [8]
(b) Draw and explain the logic diagram of BCD adder using two 4 bit adders and a correction detection circuit. [8]

UNIT-V

- Q.5 (a) Draw and explain the operation of 4 bit bidirectional shift register. [8]
(b) Write the complete steps of design of synchronous 3 bit down counter with truth tables and state diagram. [8]

OR

- Q.5 (a) Convert the S – R flip flop to J – k flip flop. [8]
(b) Sketch the logic diagram of a 4 – bit controlled buffer register and briefly explain its operation. [8]
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