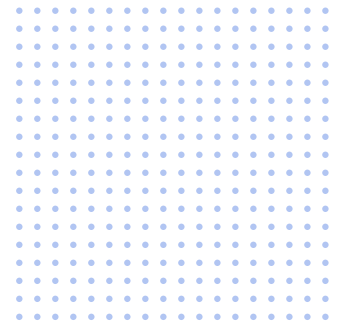




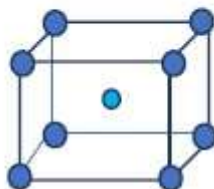
FOR JNU EE EXAM PREPARATION

JNU EE 2022 Question Paper · Ph.D Microsystems

EXAM	YEAR	TYPE	SUBJECT
JNU EE	2022	Question Paper	Ph.D Microsystems

Test Date : 09 Dec 2022**Test Slot : Slot 1****Subject : MISH-Microsystems****Sl. No.1****QBID:9152101**

The lattice structure shown in figure is:



1. Body centered cube
2. Face centered cube
3. Simple cube
4. Amorphous

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14001]

2[Option ID=14002]

3[Option ID=14003]

4[Option ID=14004]

Sl. No.2**QBID:9152102**

Si has a total of _____ electrons in its atomic structure.

1. 32
2. 14
3. 8
4. 5

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14005]

2[Option ID=14006]

3[Option ID=14007]

4[Option ID=14008]

Sl. No.3**QBID:9152103**

The alkali halide, NaCl is bonded with:

1. Ionic bonding
2. Covalent bonding
3. Metallic bonding
4. Vander-waal bonding

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14009]

2[Option ID=14010]

3[Option ID=14011]

4[Option ID=14012]

Sl. No.4

QBID:9152104

In semiconductors Si and Ge:

1. Dielectric constant of Ge > Dielectric constant of Si
2. Dielectric constant of Ge = Dielectric constant of Si
3. Dielectric constant of Ge < Dielectric constant of Si
4. Dielectric constant of Ge $\leq$ Dielectric constant of Si

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14013]

2[Option ID=14014]

3[Option ID=14015]

4[Option ID=14016]

Sl. No.5

QBID:9152105

In p-type semiconductor:

- Statement I: electrons are minority carriers, holes are majority carriers
 - Statement II: electrons are majority carriers, holes are minority carriers
1. Statement I is correct, statement II is incorrect
 2. Statement II is correct, statement I is incorrect
 3. Both the Statement I and statement II are correct
 4. Both the statement I and statement II are incorrect

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14017]

2[Option ID=14018]

3[Option ID=14019]

4[Option ID=14020]

Sl. No.6
QBID:9152106

_____ is not a trivalent p-type dopant for the Silicon semiconductor:

1. Boron
2. Gallium
3. Indium
4. Antimony

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14021]

2[Option ID=14022]

3[Option ID=14023]

4[Option ID=14024]

Sl. No.7
QBID:9152107

In reverse biased pn-junction semiconductor diode:

1. The holes in p-type move toward the junction, electrons in n-type move away from the junction
2. Both, the electrons in n-type and the holes in p-type move away from the junction
3. Holes in p-type move away from the junction, electrons in n-type move toward the junction
4. Both, the electrons in n-type and holes in p-type move toward the junction

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14025]

2[Option ID=14026]

3[Option ID=14027]

4[Option ID=14028]

Sl. No.8
QBID:9152108

A _____ barrier is formed by contacting n-type semiconductor with metal having large work function.

1. Varactor
2. Schottky
3. Parametric
4. Ohmic

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14029]

2[Option ID=14030]
 3[Option ID=14031]
 4[Option ID=14032]

Sl. No.9

QBID:9152109

Metals have electrical conductivity:

1. Less than semiconductors
2. Less than insulators
3. More than semiconductors
4. Intermediate semiconductors and insulators

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14033]
 2[Option ID=14034]
 3[Option ID=14035]
 4[Option ID=14036]

Sl. No.10

QBID:9152110

Impurities incorporated semiconductors are called:

1. Intrinsic semiconductor
2. Extrinsic semiconductor
3. Pure semiconductor
4. Dielectric

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14037]
 2[Option ID=14038]
 3[Option ID=14039]
 4[Option ID=14040]

Sl. No.11

QBID:9152111

In Si semiconductor, the value of an energy gap (a forbidden band) between conduction and valence band at 0K is:

1. 0.78eV
2. 1.21eV
3. 0.1eV
4. 1.8eV

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14041]
 2[Option ID=14042]

3[Option ID=14043]
4[Option ID=14044]

Sl. No.12
QBID:9152112

In _____, the large forbidden separates the valence band from the conduction band:

1. Metals
2. Insulators
3. Semiconductors
4. Extrinsic semiconductor

- (1) 1
(2) 2
(3) 3
(4) 4

1[Option ID=14045]
2[Option ID=14046]
3[Option ID=14047]
4[Option ID=14048]

Sl. No.13
QBID:9152113

In n-type semiconductor materials, the free electrons concentration is _____ the density of donor atoms:

1. Greater than
2. Less than
3. Approximately equal
4. Not related

- (1) 1
(2) 2
(3) 3
(4) 4

1[Option ID=14049]
2[Option ID=14050]
3[Option ID=14051]
4[Option ID=14052]

Sl. No.14
QBID:9152114

The ease with which electrons can drift in a solid material is termed as:

1. Electrons Mobility
2. Electrons Affinity
3. Electrons Excitation
4. Electrons Repulsion

- (1) 1
(2) 2
(3) 3
(4) 4

1[Option ID=14053]

2[Option ID=14054]
 3[Option ID=14055]
 4[Option ID=14056]

Sl. No.15
QBID:9152115

A constant electric field E is applied to the metal, under steady state condition, the drift velocity attained by the electrons will be in the direction _____ the electric field and it's magnitude is _____ proportional to the electric field.

1. Same as, Directly
2. Same as, Inversely
3. Opposite to, Directly
4. Opposite to, Inversely

- (1) 1
 (2) 2
 (3) 3
 (4) 4

1[Option ID=14057]
 2[Option ID=14058]
 3[Option ID=14059]
 4[Option ID=14060]

Sl. No.16
QBID:9152116

Conductivity (σ) of the sample is related with the concentration of free electrons (n_e) and mobility of the electrons μ_e , as below:

1. $\sigma = n_e \mu_e e$
2. $\sigma = n_e e / \mu_e$
3. $\sigma = e / n_e \mu_e$
4. $\sigma = n_e \mu_e$

- (1) 1
 (2) 2
 (3) 3
 (4) 4

1[Option ID=14061]
 2[Option ID=14062]
 3[Option ID=14063]
 4[Option ID=14064]

Sl. No.17
QBID:9152117

_____ process is used to grow the silicon crystal in semiconductor manufacturing industry.

1. Flat zone technique
2. Diffusion
3. Etching
4. Implantation

- (1) 1
 (2) 2

(3) 3

(4) 4

1[Option ID=14065]

2[Option ID=14066]

3[Option ID=14067]

4[Option ID=14068]

Sl. No.18**QBID:9152118**

In IC manufacturing industry, class 10 cleanroom is:

1. Less than 10 particles of size greater than 1 μ m size in each cubic cm
2. Less than 10 particles of size greater than 1 μ m size in each cubic m
3. Less than 10 particles of size greater than 0.5 μ m size in each cubic foot
4. Less than 10 particles of size greater than 0.5 μ m size in each cubic cm

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14069]

2[Option ID=14070]

3[Option ID=14071]

4[Option ID=14072]

Sl. No.19**QBID:9152119**

_____ process is used to get the pattern on the film in VLSI/MEMS technology.

1. Deposition
2. Diffusion
3. Lithography
4. Epitaxy

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14073]

2[Option ID=14074]

3[Option ID=14075]

4[Option ID=14076]

Sl. No.20**QBID:9152120**

_____ provides a very precise means to introduce a specific dose of dopants into the silicon:

1. Ion implantation
2. Deposition
3. Epitaxy
4. Etching

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14077]

2[Option ID=14078]

3[Option ID=14079]

4[Option ID=14080]

Sl. No.21**QBID:9152121**

Etch selectivity is the:

1. Etch rate of the film need to be etched / Etch rate of the mask film or photoresist
2. Etch rate of the mask film or photoresist/ Etch rate of the underlying film need to be etched
3. Etch rate of the underlying film need to be etched
4. Etch rate of the mask film

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14081]

2[Option ID=14082]

3[Option ID=14083]

4[Option ID=14084]

Sl. No.22**QBID:9152122**

In proximity printing,

- Statement I: Mask and wafer are placed separated by 5-20 μ m
 - Statement II: Mask is placed chrome side down in direct contact with the resist layer
1. Both statement I and statement II are correct
 2. Both statement I and statement II are incorrect
 3. Statement I is correct but statement II is incorrect
 4. Statement I is incorrect but statement II is correct

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14085]

2[Option ID=14086]

3[Option ID=14087]

4[Option ID=14088]

Sl. No.23**QBID:9152123**

MEMS structure is made on the top of substrate, without etching the substrate, using:

1. Bulk micromachining
2. Surface micromachining
3. Metallization process
4. Czochralski technique

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14089]

2[Option ID=14090]

3[Option ID=14091]

4[Option ID=14092]

Sl. No.24

QBID:9152124

In lithography, _____ process is used to cover the substrate/film with the photoresist.

1. Diffusion
2. Epitaxy
3. Spin coat
4. Ion implantation

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14093]

2[Option ID=14094]

3[Option ID=14095]

4[Option ID=14096]

Sl. No.25

QBID:9152125

_____ property of the polysilicon material makes it suitable for MEMS pressure sensor.

1. Piezo-resistive
2. Piezo-electric
3. Piezo-capacitive
4. Both Piezo-electric and piezo-capacitive

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14097]

2[Option ID=14098]

3[Option ID=14099]

4[Option ID=14100]

Sl. No.26

QBID:9152126

In an ideal n-MOSFET, the region of transistor operation where it acts as a resistor is :

1. Linear region of transfer I-V characteristics
2. Cut-Off region of transfer I-V characteristics
3. Saturation region of transfer I-V characteristics
4. Unstable

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14101]

2[Option ID=14102]

3[Option ID=14103]

4[Option ID=14104]

Sl. No.27

QBID:9152127

Velocity saturation and mobility degradation in n-MOSFET leads to:

1. Lower on current (I_{on}) than ideal
2. Higher on current (I_{on}) than ideal
3. Lower off current (I_{off}) than ideal
4. Higher off current (I_{off}) than ideal

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14105]

2[Option ID=14106]

3[Option ID=14107]

4[Option ID=14108]

Sl. No.28

QBID:9152128

Short channel effect starts to incur when channel length is reduced using various scaling methods. Which of the following phenomenon is NOT observed in a short channel effect?

1. Lowering of Threshold voltage (V_T roll off with decrease in channel length)
2. Drain Induced barrier lowering
3. Increase in subthreshold leakage current
4. Thermal degradation

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14109]

2[Option ID=14110]

3[Option ID=14111]

4[Option ID=14112]

Sl. No.29**QBID:9152129**

The gate level design in the following net list:

```
module Carry (input logic a, b, c,
              output logic Cout);
```

```
logic x,y,z;
```

```
and g1(x, a, b);
```

```
and g2(x, a, c);
```

```
and g3(x, b, c);
```

```
or g4(Cout, x, y, z);
```

```
end module
```

follows which of the following format?

1. Structural
2. Geometrical
3. Physical
4. Cyber Physical

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14113]

2[Option ID=14114]

3[Option ID=14115]

4[Option ID=14116]

Sl. No.30**QBID:9152130**

Static Random-Access Memory unit is most commonly present in:

1. Primary memory
2. Virtual memory
3. Cache memory
4. Secondary memory

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14117]

2[Option ID=14118]

3[Option ID=14119]

4[Option ID=14120]

Sl. No.31**QBID:9152131**

A conventional Dynamic Random-Access Memory cell is:

Statement I: slower than Static Random-Access Memory

Statement II: made up of four MOS transistors

Statement III: made up of one NMOS transistor and a MOS capacitor

Statement IV: made up of two NMOS transistors and two MOS capacitors

Which of the above-mentioned statements are correct?

1. I and III
2. I only
3. I and II
4. I and IV

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14121]

2[Option ID=14122]

3[Option ID=14123]

4[Option ID=14124]

Sl. No.32

QBID:9152132

Which of the following memory element is the fastest?

1. Dynamic Random Access Memory
2. Static Random Access Memory
3. Both Dynamic and Static Random Access Memory
4. Registers

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14125]

2[Option ID=14126]

3[Option ID=14127]

4[Option ID=14128]

Sl. No.33

QBID:9152133

The number of MOS transistors required to design a Multiplexer can be reduced by replacing it with:

1. n-type Metal Oxide Semiconductor Field Effect Transistor
2. p-type Metal Oxide Semiconductor Field Effect Transistor
3. Transmission Gate
4. Pass transistor

(1) 1

(2) 2

(3) 3

(4) 4

- 1[Option ID=14129]
 2[Option ID=14130]
 3[Option ID=14131]
 4[Option ID=14132]

Sl. No.34
QBID:9152134

Which of the following statement is true for p-Type Metal Oxide Semiconductor Field Effect Transistor ?

1. It is good in passing "Zero" but bad in passing "1"
2. It is good in passing "1" but bad in passing "0"
3. It is good in passing both "Zero" and "1"
4. It is bad in passing both "Zero" and "1"

- (1) 1
 (2) 2
 (3) 3
 (4) 4

- 1[Option ID=14133]
 2[Option ID=14134]
 3[Option ID=14135]
 4[Option ID=14136]

Sl. No.35
QBID:9152135

In a CMOS based circuit, n-type Metal Oxide Semiconductor Field Effect Transistor acts as

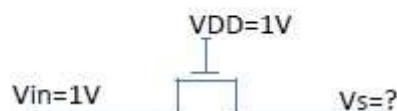
1. Pull up Network
2. Pull down Network
3. Both as a Pull up Network and a Pull-down Network
4. Load

- (1) 1
 (2) 2
 (3) 3
 (4) 4

- 1[Option ID=14137]
 2[Option ID=14138]
 3[Option ID=14139]
 4[Option ID=14140]

Sl. No.36
QBID:9152136

The value at V_s for the following n-MOSFET circuit configuration, where $V_{Tn}=0.4V$ is:



1. 0V
2. 0.6V
3. 1V
4. 1.4V

- (1) 1
(2) 2
(3) 3
(4) 4

1[Option ID=14141]

2[Option ID=14142]

3[Option ID=14143]

4[Option ID=14144]

Sl. No.37

QBID:9152137

In a n-MOSFET (enhancement mode), the applied gate voltage to form the inversion layer is:

1. Positive and higher or equal to the threshold voltage
2. Negative and lower or equal to the threshold voltage
3. Inversion layer already exist
4. Inversion layer never formed

- (1) 1
(2) 2
(3) 3
(4) 4

1[Option ID=14145]

2[Option ID=14146]

3[Option ID=14147]

4[Option ID=14148]

Sl. No.38

QBID:9152138

In a n-substrate MOS capacitor, the total capacitance is due to:

1. Depletion layer Capacitance
2. Insulator Capacitance
3. Depletion layer Capacitance in series with the Insulator Capacitance
4. Depletion layer Capacitance in parallel with the Insulator Capacitance

- (1) 1
(2) 2
(3) 3
(4) 4

1[Option ID=14149]

2[Option ID=14150]
 3[Option ID=14151]
 4[Option ID=14152]

Sl. No.39
QBID:9152139

If a MOSFET is scaled down by a factor of k (i.e. Both horizontal and vertical dimensions are scaled by a factor of k along with voltage which is also scaled down by a factor of k to keep the internal electric field constant), the new transconductance shall modify by a factor of :

1. k
2. $1/k$
3. $1/k^2$
4. 1

- (1) 1
 (2) 2
 (3) 3
 (4) 4

1[Option ID=14153]
 2[Option ID=14154]
 3[Option ID=14155]
 4[Option ID=14156]

Sl. No.40
QBID:9152140

Number of NAND gates required to implement Exclusive-OR operation:

1. One
2. Two
3. Three
4. Four

- (1) 1
 (2) 2
 (3) 3
 (4) 4

1[Option ID=14157]
 2[Option ID=14158]
 3[Option ID=14159]
 4[Option ID=14160]

Sl. No.41
QBID:9152141

A _____ is sensitive to pulse duration.

1. Latch
2. Flip flops
3. Both Latch and Flip Flop
4. Multiplexer

- (1) 1
 (2) 2

(3) 3

(4) 4

1[Option ID=14161]

2[Option ID=14162]

3[Option ID=14163]

4[Option ID=14164]

Sl. No.42**QBID:9152142**

How many Flip Flops must be complemented in a 10-bit binary ripple counter to reach the next count after 0111111111?

1. One
2. Five
3. Ten
4. Eight

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14165]

2[Option ID=14166]

3[Option ID=14167]

4[Option ID=14168]

Sl. No.43**QBID:9152143**

Complementary Metal Oxide Semiconductor (CMOS) based circuits are preferred over n-MOSFET circuits due to it's _____

1. Higher voltage gain
2. Higher Current gain
3. Lower leakage current
4. Higher voltage gain and higher current gain

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14169]

2[Option ID=14170]

3[Option ID=14171]

4[Option ID=14172]

Sl. No.44**QBID:9152144**

Latch up phenomenon in a CMOS Process occurs due to _____.

1. "Turning ON" of Parasitic bipolar transistor formed by the Substrate, Well and diffusion.
2. "Turning OFF" of Parasitic bipolar transistor formed by the Substrate, Well and diffusion.
3. "Turning OFF" of Parasitic Capacitance in the CMOS process.
4. "Turning ON" of Parasitic Capacitance in the CMOS process.

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14173]

2[Option ID=14174]

3[Option ID=14175]

4[Option ID=14176]

Sl. No.45**QBID:9152145**

The Boolean function for two outputs of a half subtractor are (where D = Difference and B = Borrow):

1. $D = x'y' + x'y$; $B = x'y'$

2. $D = x'y' + x'y$; $B = xy'$

3. $D = x'y + xy'$; $B = x'y'$

4. $D = x'y + xy'$; $B = x'y$

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14177]

2[Option ID=14178]

3[Option ID=14179]

4[Option ID=14180]

Sl. No.46**QBID:9152146**

D flip flop is _____

1. Modification of latch
2. Modification of clocked RS flip flop
3. Modification of clocked JK flip flop
4. Modification of clocked T flip flop

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14181]

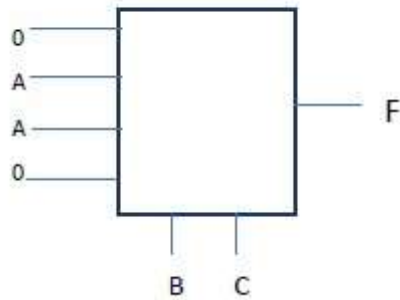
2[Option ID=14182]

3[Option ID=14183]

4[Option ID=14184]

Sl. No.47**QBID:9152147**

The output F of the 4X1 Multiplexer is:



1. $F=A.(B+C)$
2. $F=A+B+C$
3. $F=A.(B\oplus C)$
4. $F=A\oplus B\oplus C$

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14185]

2[Option ID=14186]

3[Option ID=14187]

4[Option ID=14188]

Sl. No.48

QBID:9152148

Conversion of octal digit $(72.22)_8$ to a binary

1. $(111011.001010)_2$
2. $(111010.010010)_2$
3. $(11111011.11001011)_2$
4. $(11110111.00101000)_2$

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14189]

2[Option ID=14190]

3[Option ID=14191]

4[Option ID=14192]

Sl. No.49

QBID:9152149

The number of NOR gates required to implement OR operation would be :

1. One
2. Two
3. Three
4. Four

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14193]

2[Option ID=14194]

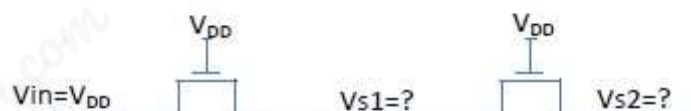
3[Option ID=14195]

4[Option ID=14196]

Sl. No.50

QBID:9152150

In n-MOSFET circuit configuration shown below:



Which of the following is true? (Neglect the body effect).

1. $V_{s1} < V_{s2}$
2. $V_{s1} > V_{s2}$
3. $V_{s1} = V_{s2} = V_{DD} - V_{Tn}$
4. $V_{s1} = V_{s2} = V_{DD} - 2V_{Tn}$

(1) 1

(2) 2

(3) 3

(4) 4

1[Option ID=14197]

2[Option ID=14198]

3[Option ID=14199]

4[Option ID=14200]